The Claims:

1. (Previously Presented) A node comprising:

a motherboard;

a switch comprising eight or more ports, the switch integrated on the motherboard; and

at least two processors, each processor communicably coupled to the integrated switch and integrated on the motherboard.

2. (Previously Presented) The node of Claim 1, each processor coupled to the integrated switch through a Host Channel Adapter (HCA).

3. (Previously Presented) The node of Claim 2, each processor further coupled to the integrated switch through a peripheral component interconnect (PCI) bridge.

4. (Previously Presented) The node of Claim 1, at least two of the processors communicably coupled directly to each other via a link supporting processor-to-processor communication.

5. (Previously Presented) The node of Claim 1, each processor communicably coupled to the integrated switch through a Northbridge.

6. (Currently Amended) The node of Claim 1, the integrated switch operable to communicate input/output (I/O) messages at a bandwidth ~~substantially similar to power~~ that is approximately equal to a processing speed of the processors.

7. (Previously Presented) The node of Claim 1, the integrated switch comprising twenty-four ports and enabling a toroidal topology comprising four dimensions.

8. (Previously Presented) The node of Claim 1, the integrated switch operable to:

communicate a first message from a first of the two or more processors; and

communicate a second message from a second of the two or more processors, the first and second message communicated in parallel.

9. (Previously Presented) A system comprising a plurality of interconnected nodes, each node comprising:

a motherboard;

a switch comprising eight or more ports, the switch integrated on the motherboard and operable to interconnect at least a subset of the plurality of nodes; and

at least two processors, each processor communicably coupled to the integrated switch and integrated on the motherboard.

10. (Previously Presented) The system of Claim 9, the two or more processors on each node coupled to the integrated switch through a Host Channel Adapter (HCA).

11. (Previously Presented) The system of Claim 10, the two or more processors on each node further coupled to the integrated switch through a peripheral component interconnect (PCI) bridge.

12. (Previously Presented) The system of Claim 9, wherein, on each of one or more of the nodes, at least two of the processors on the node are communicably coupled directly to each other via a link supporting processor-to-processor communication.

13. (Previously Presented) The system of Claim 9, the two or more processors on each node communicably coupled to the integrated switch through a Northbridge.

14. (Currently Amended) The system of Claim 9, the integrated switch of each node operable to communicate input/output (I/O) messages at a bandwidth ~~substantially similar to power~~ that is approximately equal to a processing speed of the processors.

15. (Previously Presented) The system of Claim 9, the integrated switch of each node comprising twenty-four ports and enabling a toroidal topology comprising four dimensions.

16. (Previously Presented) The system of Claim 9, the plurality of nodes arranged in a topology, the topology enabled by the integrated fabric of each node.

17. (Previously Presented) The system of Claim 16, the topology comprising a hypercube.

18. (Previously Presented) The system of Claim 16, the topology comprising a folded topology.

19. (Previously Presented) The system of Claim 9, a first node of the plurality of nodes interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis that is perpendicular to the X axis, a fourth node of the plurality of nodes along a Z axis that is perpendicular to the X and Y axes, and a fifth node along a diagonal axis that is oblique to one or more of the X, Y, and Z axes.

20. (Previously Presented) The system of Claim 19, the connection between the first node and the fifth node operable to reduce message jumps among the plurality of nodes.

21. (Previously Presented) A method for forming a node, comprising:

providing a motherboard;

integrating a switch with the motherboard, the integrated switch comprising eight or more ports;

integrating at least two processors with the motherboard; and

coupling each processor with the integrated switch.

22. (Original) The method of Claim 21, wherein coupling each processor with the integrated switch comprises coupling each processor to the integrated switch through a Host Channel Adapter (HCA).

23. (Previously Presented) The method of Claim 22, wherein coupling each processor with the integrated switch comprises coupling each processor to the integrated switch through a peripheral component interconnect (PCI) bridge.

24. (Previously Presented) The method of Claim 21, further comprising coupling at least two of the processors directly to each other via a link supporting processor-to-processor communication.

25. (Previously Presented) The method of Claim 21, wherein coupling each processor with the integrated switch comprises coupling each processor communicably to the integrated switch through a Northbridge.

26. (Currently Amended) The method of Claim 21, the integrated switch operable to communicate input/output (I/O) messages at a bandwidth ~~substantially similar to power~~ that is approximately equal to a processing speed of the processors.

27. (Previously Presented) The method of Claim 21, the integrated switch comprising twenty-four ports and enabling a toroidal topology comprising four dimensions.